Digital Electronics Lab 2021310

Sr. No	List of experiment	E Content
1	To verify the truth tables for all logic gates – NOT OR AND NAND NOR XOR XNOR using CMOS Logic gates and TTL Logic Gates.	https://de-iitr.vlabs.ac.in/exp/truth-table-gates/theory.html
2	Implement and realize Boolean Expressions with Logic Gates	https://dec-iitkgp.vlabs.ac.in/exp/basic-logic-gates/theory.html
3	Implement Half Adder, Full Adder, Half Subtractor, Full Subtractor using ICs	https://de-iitr.vlabs.ac.in/exp/half-full-subtractor/
4	Implement parallel and serial full-adder using ICs	http://vlabs.iitkgp.ernet.in/dec/exp7/index.html
5	Design and development of Multiplexer and De-multiplexer using multiplexer ICs	https://de-iitr.vlabs.ac.in/exp/multiplexer-demultiplexer/theory.html
6	Verification of the function of SR,D, JK and T Flip Flops	https://de-iitr.vlabs.ac.in/exp/truth-tables-flip-flops/
7	Design controlled shift registers	https://de-iitr.vlabs.ac.in/exp/4bit-sipo-shift-register/theory.html
8	Study Digital- to – Analog and Analog to Digital Converters	https://he-coep.vlabs.ac.in/exp/digital-analog-converter/theory.html